REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-20 are pending in the present application. Claims 1, 8, and 14 have been amended.

II. Claim Amendments

Independent claims 1, 8, and 14 have been amended to recite that the obtaining of the "set of timing and relation criteria is dependent on at least one of when a packet should be transmitted, how long it should take to transmit the packet, and a relation of the packet to other packets." No new matter has been added by way of these amendments as support for these amendments may be found, for example, on page 5, line 22 – page 6, line 8 of the present application.

III. Rejection(s) Under 35 U.S.C § 103

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,937,182 issued to Allingham (hereinafter "Allingham") in view of U.S. Patent No. 6,324,665 issued to Fay (hereinafter "Fay"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a sequence-based verification method and

system for verifying the functionality of hardware components that move data between nodes in a computer system. The verification method involves generating a set of packets, each of which includes data to be transmitted from one node in the computer system to another node. Each packet also includes information such as when the data should be transmitted, how long it should take to transmit the data, how the packet relates to the other packets, etc. Using the information contained in the packets, timing and relation criteria are determined. The timing and relation criteria determine the sequence in which the packets should be transmitted. Using the predetermined sequence, the verification system presents the packets to a hardware component for transmission. The verification system then monitors the output of the hardware component to determine whether the predetermined sequence is preserved. *See* Specification, page 5, line 22 – page 6, line 8.

As described in the present application, drive modules, or drive loops, fill drive buffers with packets of data that are to be driven by a device under test. *See* Specification, page 8, lines 5 – 10. Using information contained in the packets, a timing sequence is determined by which the packets are to be driven by the device under test. *See* Specification, page 8, line 23 – page 9, line 9. This sequence is also stored in expect buffers that are used to subsequently check whether the driving of packets by the device under test conformed to the timing sequence. *See* Specification, page 11, line 24 – page 12, line 8. Accordingly, the verification method of the present invention is sequence-based, where the sequence, as recited in amended independent claims 1, 8, and 14 of the present application, is determined dependent on at least one of when a packet should be transmitted, how long it should take to transmit the packet, and a relation of the packet to

other packets. *See* Specification, page 5, line 22 – page 6, line 8.

With respect to Allingham, the Examiner specifically states that Allingham fails to obtaining timing and relation criteria are obtained that determine the sequence in which the packets should be driven as well as confirming that the timing and relation criteria are satisfied prior to allowing the drive loop to force the device under to test to drive the packets. *See* Office Action of July 8, 2003, page 4. Fay also fails to teach these limitations.

Fay is directed to testing a device under test by comparing events measured on a known good device under test with event measured on a potentially faulty device under test. *See* Fay, Abstract. The portions of Fay cited by the Examiner disclose that event lists for a potentially faulty device under test are time aligned and compared with event lists for a known good device under test to determine whether the potentially faulty device under test is actually faulty. However, the cited portions of Fay, or any other portion of Fay, fail to disclose determining a sequence by which to drive packets of data dependent on at least one of when a packet should be transmitted, how long it should take to transmit the packet, and a relation of the packet to other packets as required by amended independent claims 1, 8, and 14 of the present application. In other words, Fay is altogether silent as to the determination of a sequence by which to have data propagated.

In view of the above, Allingham and Fay, whether considered separately or in combination, fail to show or suggest the present invention as recited in amended independent claims 1, 8, and 14 of the present application. Thus, amended independent claims 1, 8, and 14 of the present application are patentable over Allingham and Fay.

Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV.   Conclusion

Applicant believes this reply to be fully responsive to all outstanding issues and place this application in condition for allowance. If this belief is incorrect, or other issues arise, do not hesitate to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 06145.012001;P4860).

Respectfully submitted,

Date: _8/25/03_

Jonathan P. Osha, Reg. No. 33,986
ROSENTHAL & OSHA L.L.P.
1221 McKinney Street, Suite 2800
Houston, TX 77010

Telephone: (713) 228-8600
Facsimile: (713) 228-8778

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